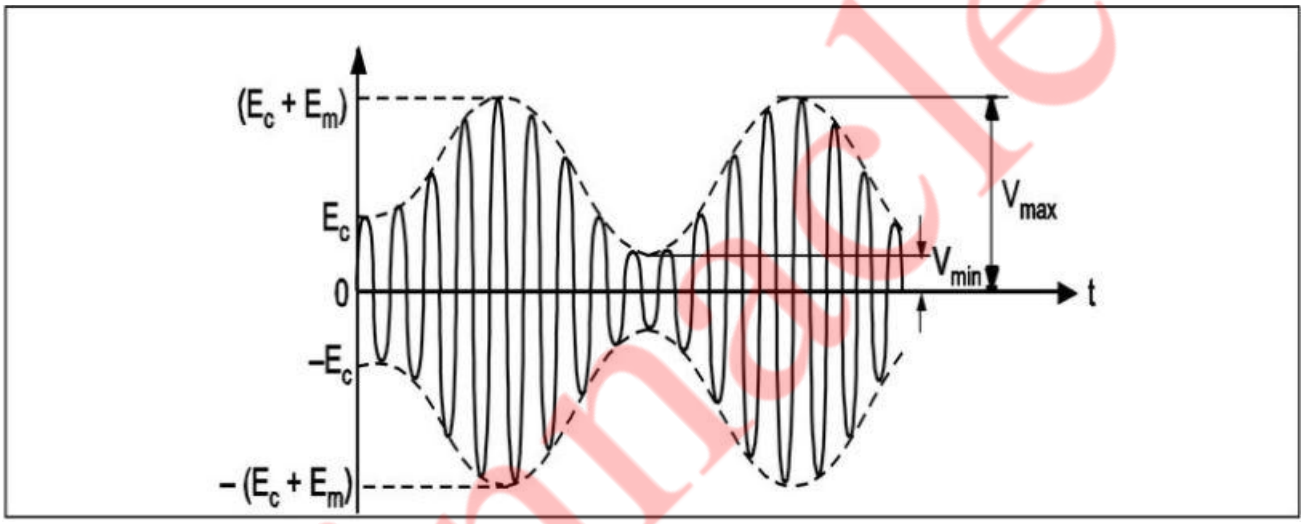
Electronic circuits and communication fundamentals (ECCF)

Dec-2019(Choice based)

Q1 A) Represent an AM signal both in time domain and frequency domain giving their mathematical equation for eAM. (5)

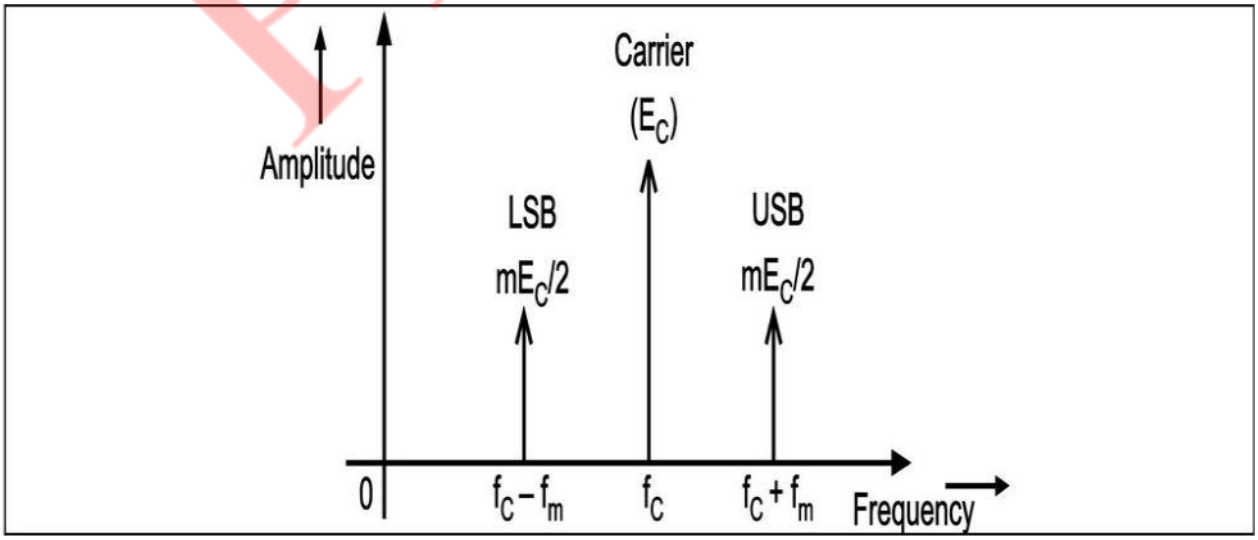
Solution:

AM signal in time domain



eAM = (EC + Em Sin ωmt) Sin ωct

AM signal in frequency domain



$$eAM = Ec \sin \omega ct + \frac{mEc}{2} \cos(\omega c - \omega m)t - \frac{mEc}{2} \cos(\omega c + \omega m)$$

Q1 B) List ideal and practical characteristics with their value for op-amp. (5)

Solution:

Ideal Op – Amp is a device which holds the following characteristics:

1. It has infinite voltage gain.

2. It has zero offset voltage. That is, the zero output voltage obtained in Op – Amp even for the zero differential input voltage.

3. It has infinite bandwidth.

4. It has zero output impedance.

5. It has infinite input impedance.

But practically these are not possible due to the imperfections in the manufacturing of practical Op – Amp.

Practical Op – Amp holds the following characteristics:

1. The open loop gain of practical Op – Amp is around 7000.

2. Practical Op – Amp has non zero offset voltage. That is, the zero output is obtained for the non – zero differential input voltage only.

3. The bandwidth of practical Op – Amp is very small value. This can be increased to desired value by applying an adequate negative feedback to the Op – Amp.

4. The output impedance is in the order of hundreds. This can be minimized by applying an adequate negative feedback to the Op – Amp.

5. The input impedance is in the order of Mega Ohms only. (Whereas the ideal Op – Amp has infinite input impedance).

Q1 C) What is Dc load line? What is the importance of Q-point selection on a DC load line? (5)

Solution:

When the transistor is given the bias and no signal is applied at its input, the load line drawn under such conditions, can be understood as DC condition.

Here there will be no amplification as the signal is absent. This condition off amplifier is known as Quiscent condition, where only Dc voltage are applied.

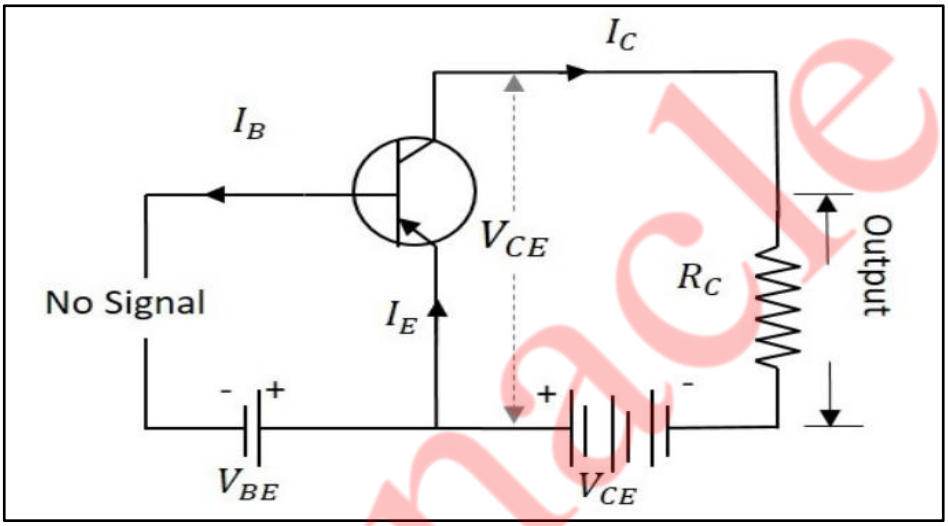


Fig1: Circuit diagram for DL

The value of collector emitter voltage at any given time will be

VCE=VCC−IC RC

As VCC and RC are fixed values, the above one is a first degree equation and hence will be straight line on the output characteristics. This line is called as D.C Load line.This line can be drawn on o/p characteristics of CE.

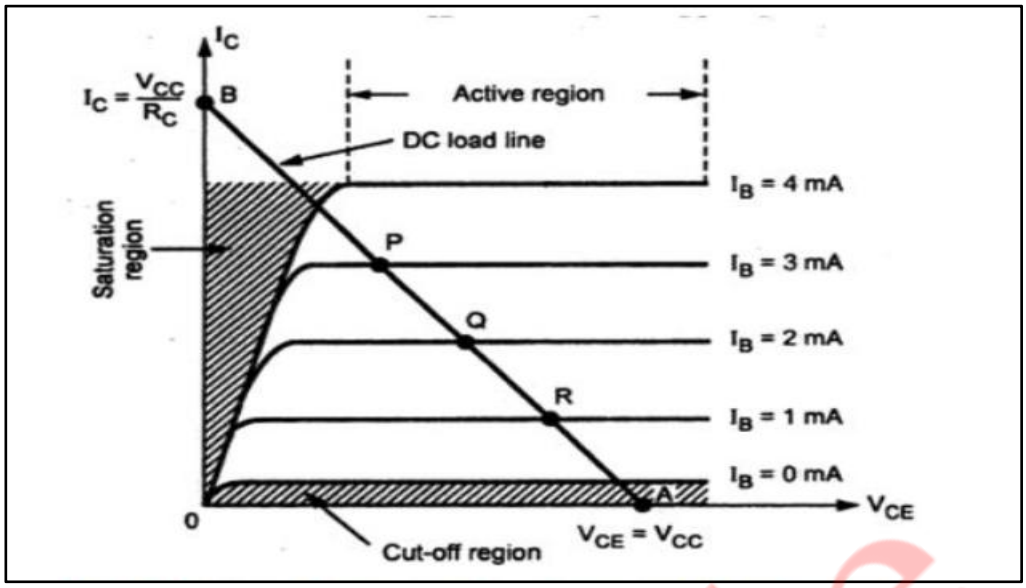


Fig2: Common emitter output characteristics with dc load line

A point can be obtained on DC load line which is called Q-point.

Normally whatever signals we want to amplify will be of the order milli volts or less. If we directly input these signals to the amplifier they will not get amplified as transistor needs voltages greater than cut in voltages for it to be in active region. Only in active region of operation transistor acts as amplifier.

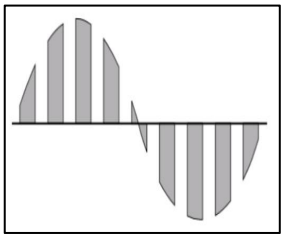
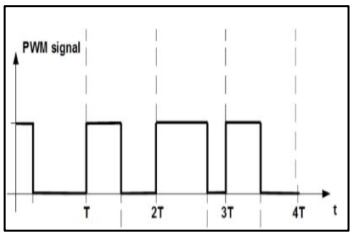
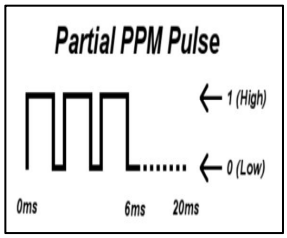
So we can establish appropriate DC voltages and currents through BJT by external sources so that BJT operates in active region and superimpose the AC signals to be amplified.

The DC voltage and current are so chosen that the transistor remains in active region for entire AC signal excursion. All the input AC signals variations happen around Q-point.

Q1 D)What are the differences between PAM, PWM and PPM. **(5)**

Solution:

Parameter	**PAM**	**PWM**	**PPM**
Type of Carrier	Train of Pulses	Train of Pulses	Train of Pulses
Variable Characteristic of the Pulsed Carrier	Amplitude	Width	Position
Bandwidth Requirement	Low	High	High
Noise Immunity	Low	High	High
Information Contained in	Amplitude Variations	Width Variations	Position Variations
Power efficiency (SNR)	Low	Moderate	High
Transmitted Power	Varies with amplitude of pulses	Varies with variation in width	Remains Constant
Complexity of generation and detection	Complex	Easy	Complex
Transmitter power	Instantaneous transmitter power varies with the amplitude of the pulses	Instantaneous transmitter power varies with the amplitude and width of the pulses	Instantaneous transmitter power remains constant with the width of the pulses

Output Waveforms			

Q2 A) Explain with neat diagram, the working of Hartley Oscillator using transistor. (10)

Solution:

In a Hartley oscillator the oscillation frequency is determined by a tank circuit comprising of two inductors and one capacitor. The inductors are connected in series and the capacitor is connected across them in parallel. Hartley oscillators are commonly used in radio frequency (RF) oscillator applications and the recommended frequency range is from 20KHz to 30MHz. Hartley oscillators can be operated at frequencies lower than 20KHz, but for lower frequencies the inductor value need to be high and it has a practical limit. The circuit diagram of a typical Hartley oscillator is shown in the figure below.

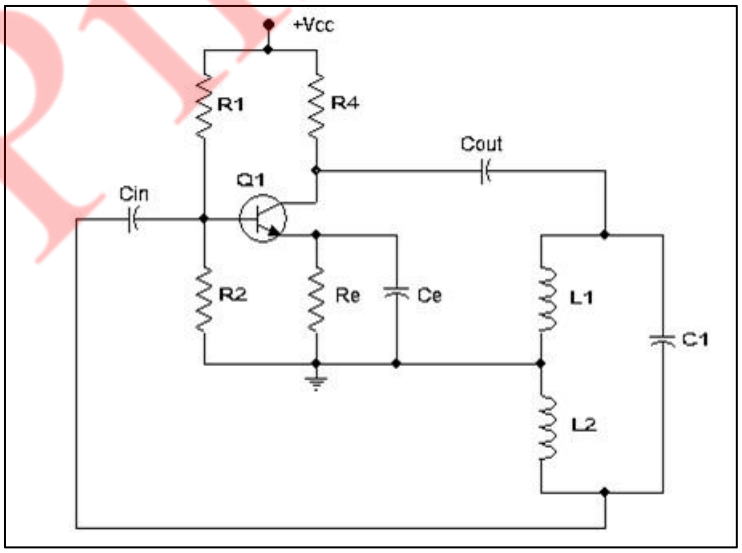


Fig1: Hartley Oscillator

In the circuit diagram resistors R1 and R2 give a potential divider bias for the transistor Q1. Re is the emitter resistor, whose job is to provide ot there, the amplified ac voltages will drop across Re and it

will get added on to the base-emitter voltage of Q1 and will disrupt the biasing conditions. Cin is the input DC decoupling capacitor while Cout is the output DC decoupling capacitor. The task of a DC decoupling capacitor is to prevent DC voltages from reaching the succeeding stage. Inductor L1, L2 and capacitor C1 forms the tank circuit.

When the power supply is switched ON the transistor starts conducting and the collector current increases. As a result the capcitor C1 starts charging and when the capacitor C1 is fully charged it starts discharging through coil L1. This charging and discharging creates a series of damped oscillations in the tank circuit and it is the key.

The oscillations produced in the tank circuit is coupled (fed back) to the base of Q1 and it appears in the amplified form across the collector and emitter of the transistor. The output voltage of the transistor (voltage across collector and emitter) will be in phase with the voltage across inductor L1. Since the junction of two inductors is grounded, the voltage across L2 will be 180° out of phase to that of the voltage across L1. The voltage across L2 is actually fed back to the base of Q1. From this we can see that, the feed back voltage is 180° out of phase with the transistor and also the transistor itself will create another 180° phase difference. So the total phase difference between input and output is 360° and it is very important condition for creating sustained oscillations.

The frequency "F" of a Hartley oscillator can be expressed using the equation;

$$F = \frac{1}{2\pi\sqrt{LC}}$$

C is the capacitance of the capacitor C1 in the tank circuit.

L = L1+L2, the effective series inductance of the inductors L1 and L2 in the tank circuit.

Here the coils L1 and L2 are assumed to be winded on different cores. If they are winded on a single core then L=L1+L2+2M where M is the mutual inductance between the two coils.

Q2 B) Describe the working of class A and class C Amplifier in detail with relevant diagrams. (10)

Solutions:

Class A Amplifier

A Class A power amplifier is one in which the output current flows for the entire cycle of the AC input supply. Hence the complete signal present at the input is amplified at the output. The purpose of the class A bias is to make the amplifier relatively free from noise by making the signal waveform out of the region between 0v to 0.6v where the transistor's input characteristic is non-linear. The following figure shows the circuit diagram for Class A Power amplifier.

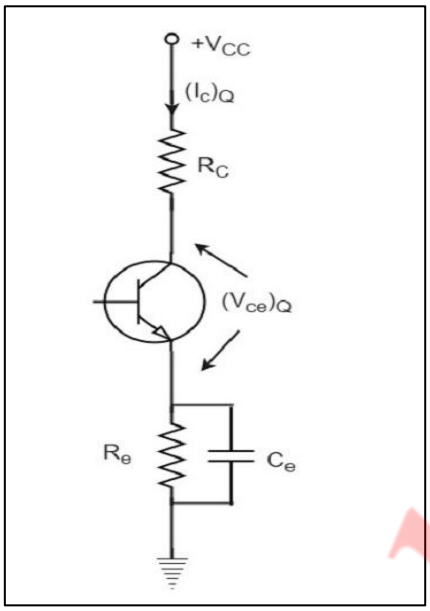


Fig1: Class A Amplifier

From the above figure, it can be observed that the transformer is present at the collector as a load. The use of transformer permits the impedance matching, resulting in the transference of maximum power to the load e.g. loud speaker.

The operating point of this amplifier is present in the linear region. It is so selected that the current flows for the entire ac input cycle. The below figure explains the selection of operating point.

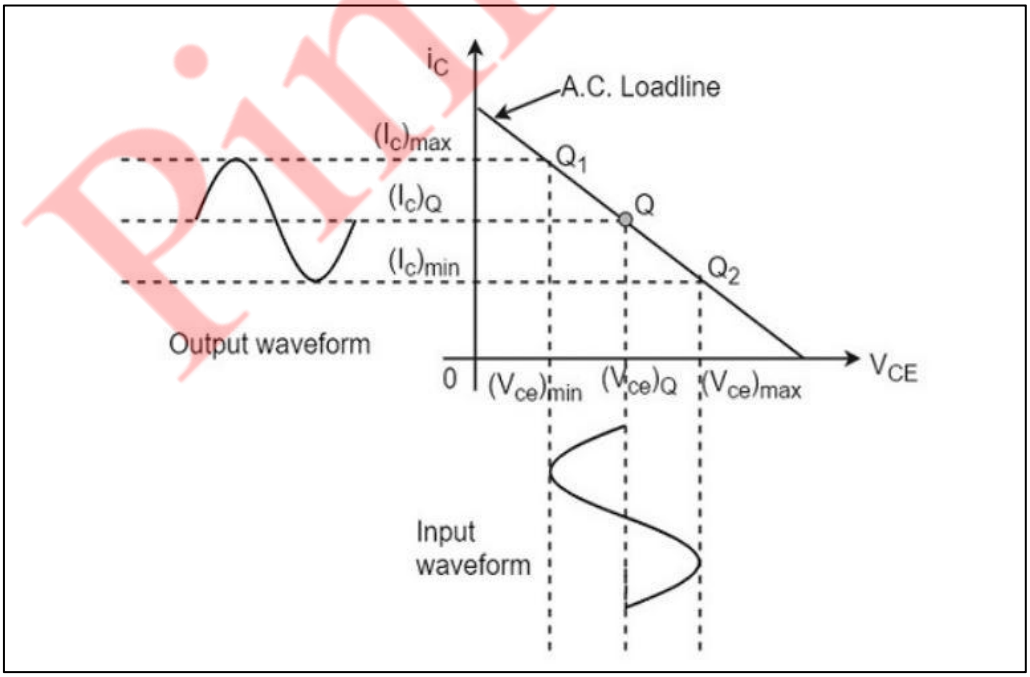


Fig2: Selection of Q-point

The output characteristics with operating point Q is shown in the figure above. Here (Ic)Q and (Vce)Q represent no signal collector current and voltage between collector and emitter respectively. When signal is applied, the Q-point shifts to Q1 and Q2. The output current increases to (Ic)max and

decreases to (Ic)min. Similarly, the collector-emitter voltage increases to (Vce)max and decreases to (Vce)min.

D.C. Power drawn from collector battery Vcc is given by

Pin=voltage×current=VCC(IC)Q

This power is used in the following two parts −

1)Power dissipated in the collector load as heat is given by

PRC=(current)2×resistance=(IC)2QRC

2)Power given to transistor is given by

Ptr=Pin−PRC=VCC−(IC)2QRC

Class C Amplifier:

Class C Amplifier is a highly efficient amplifier. During a Class C amplifier operation, the collector flows for less than half cycle of AC signal. A class C amplifier is bias for operation for less than 180° of the input signal cycle and its value is 80° to 120°.

Less than 180° (half cycle) means less than 50% and would operate only with a tuned or resonant circuit, which provides a full cycle of operation for the tuned or resonant frequency. There is a trade-off between efficiency and distortion as the efficiency improves at a large extended level by reduced conduction angle. However, it also leads to a lot of distortion. The Class C amplifiers used in RF transmitters usually are operating at a single fixed carrier frequency.In such applications, the distortion is controlled by a tuned load on the amplifiers. The input signal is applied to switch the active device (transistor) and so the current is directed to flow through a tuned load.

Working:

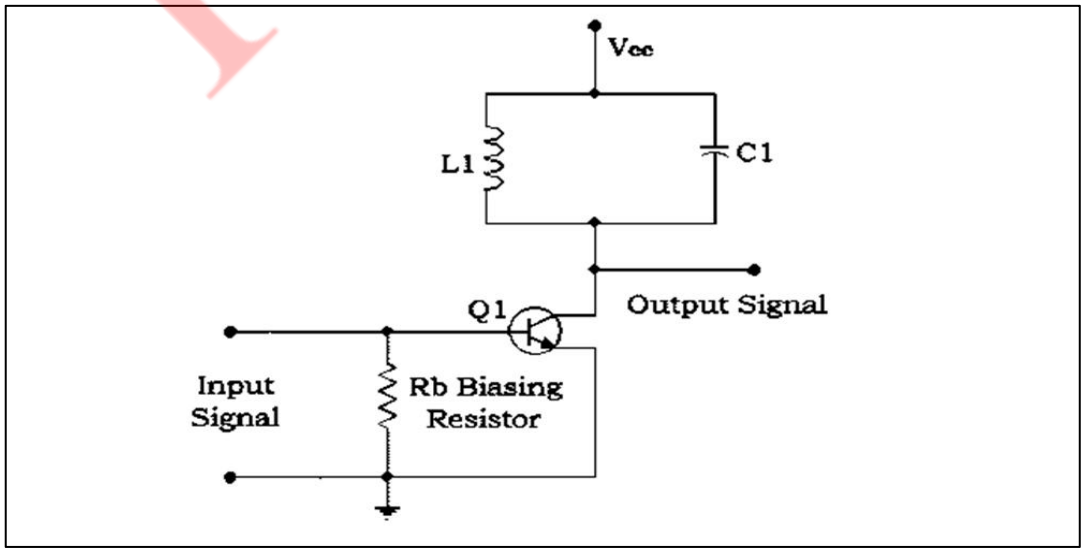


Fig 3:Class C Amplifier

As shown in the above circuit diagram, Resistor Rb connects to the transistor Q1 base. A biasing resistor which connects to the base of Q1 try to pulls the base of transistor further downwards and set

the operating pointer dc bias point below the cut-off point (In cutoff the collector current is I_{CO} which will be of micro amperes order and hence can be assumed to be zero) in the DC load line. The dc load line is the locus of IC and VCE at which BJT remains in active region.

The reason for the major portion of the input signal is absent in the output signal is that the transistor will start conducting only after the input signal amplitude has risen above the base emitter voltage (Vbe~0.7V) and according to the result the downward bias voltage caused by Rb.

As shown in Fig 3, inductor L1 and capacitor C1 forms a tuned circuit which is also called a tank circuit. LC circuits are used either for generating signals at a particular frequency, or picking out a signal at a particular frequency from a more complex signal which extract the required signal from the pulsed output of the transistor.

A series of current pulses is produced by the transistor (active element) according to the input which flow through the resonant circuit. The tank circuit oscillates in the frequency of the input signal by selecting the proper value of L and C. All other frequencies are attenuated by tank circuit and the tank circuit oscillates in one frequency.

The required frequency is obtained by using a suitably tuned load. The output signal noise can be eliminated by using additional filters. For transferring the power to the load from the tank circuit, a coupling transformer is used.

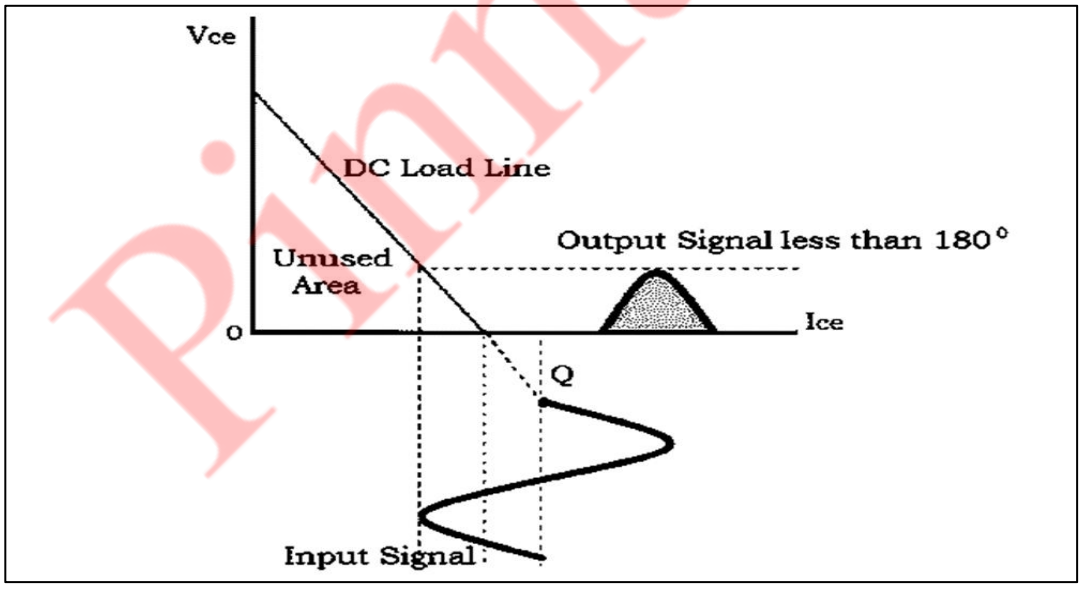


Fig4:Operating Point

As shown in Fig 4, it can be observed that the operating point is placed some way below the cut-off point in the DC load-line and so only a fraction of the input waveform is available at the output.

Q3 A) Explain the application of op-amp as differentiator. (10)

Solution:

Differentiator is a circuit which provides an o/p waveform whose value at any instant of time is equal to the rate of input at that point in time.

Differentiator is a circuit which produce o/p voltage which is derivative of i/p voltage.

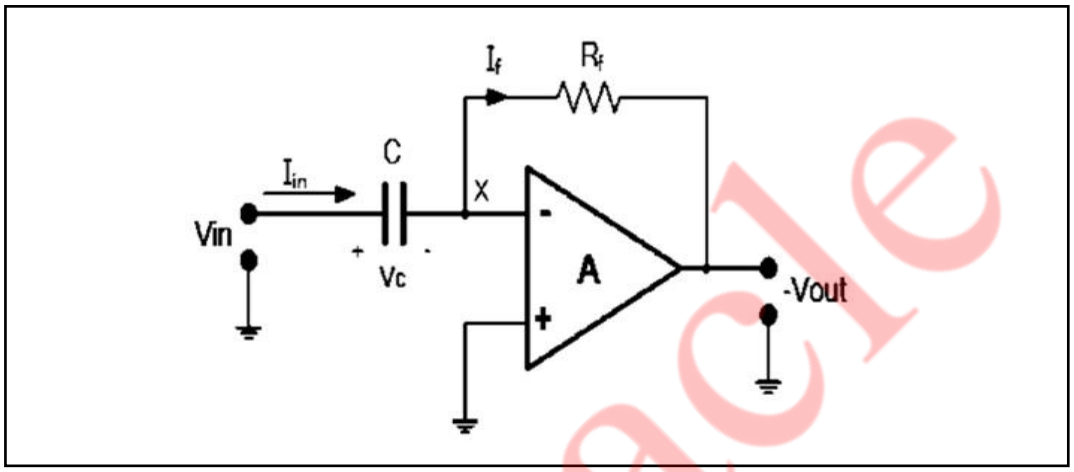


Fig: Op-amp Differentiator circuit

The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, X resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependant on the rate of change of the input signal.

At low frequencies the reactance of the capacitor is "High" resulting in a low gain (Rf/Xc) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

However, at high frequencies an op-amp differentiator circuit becomes unstable and will start to oscillate. This is due mainly to the first-order effect, which determines the frequency response of the op-amp circuit causing a second-order response which, at high frequencies gives an output voltage far higher than what would be expected. To avoid this the high frequency gain of the circuit needs to be reduced by adding an additional small value capacitor across the feedback resistor Rf.

Since the node voltage of the operational amplifier at its inverting input terminal is zero, the current, i flowing through the capacitor will be given as:

Iin = If

And If $= -\frac{Vout}{R_f}$

The charge on the capacitor

Q = C x Vin

Thus rate of change of this charge is: $\frac{dQ}{dt} = C\frac{dv_{in}}{dt}$

But dQ/dt is the capacitor current, I

IIN= $C\frac{dv_{in}}{dt}$ = IF

Therefore $-\frac{Vout}{R_f} = C\frac{dv_{in}}{dt}$

From which we have ideal voltage output for the op-amp differentiator is given as:

VOUT = -RF $C\frac{dv_{in}}{dt}$

Op-amp differentiator waveform

If we apply a constantly changing signal such as a Square-wave, Triangular or Sine-wave type signal to the input of a differentiator amplifier circuit the resultant output signal will be changed and whose final shape is dependant upon the RC time constant of the Resistor/Capacitor combination.

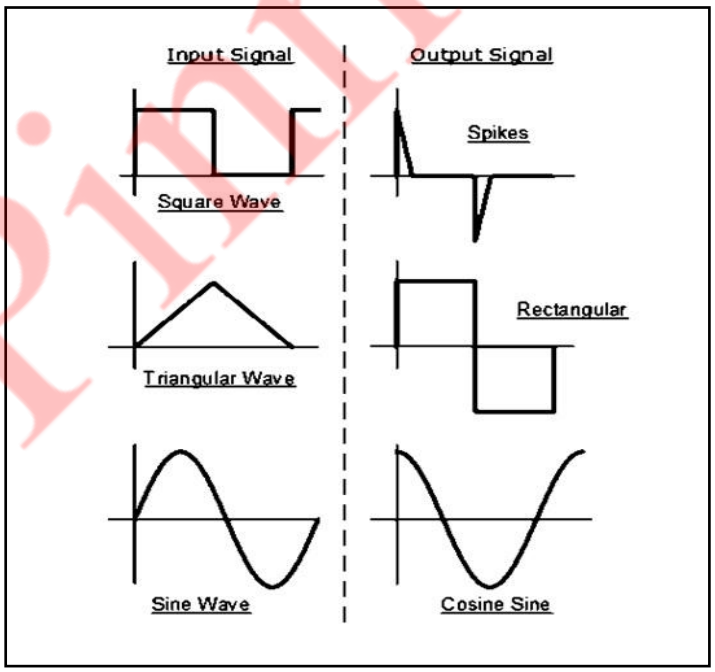


Fig2: Op-amp differentiator waveform

Q3 B) Explain the need of biasing and stabilization. In a Silicon transistor circuit with a fixed bias, Vcc=9V, Rc=0.5 KΩ, RB=60 KΩ, VBE= 0.7 V. Find the operating point on DC loa line.

(10)

Solution:

Need for biasing:

Biasing is nothing but making use of resistors and power supply connected in such a way that to obtain collector emitter voltage and collector current.

The need of providing dc biasing for transistor is to obtain a dc collector current at a certain dc collector emitter voltage.

These values of current and voltage are expressed by the term called as operating point or quiescent point.

To obtain the operating point we have to use some circuits, these circuits are called biasing circuits. So that while fixing operating point, it should provide proper dc conditions so that specific function is achieved.

Transistor operates in four different regions i.e Cutoff, Forward Active, Saturation, Inverse Active.

Need for Stabilization:

When the temperature changes or the transistor is replaced the operating point also changes.however for faithful amplification,the operating point must be remains fixed.this necessity to make the operating point independent of these variations.the process of making operating point independent of temperature changes or variations in transistor parameters is known as stablization.

The following are the factors that effect the stability of the operating point.

1) Temperature dependence of Ic.

2) Change of VBE and β due to replacement of transistor.

3) Thermal runway.

Given:

Vcc=9V,

Rc=0.5 KΩ,

RB=60 KΩ,

VBE= 0.7 V.

Ic= $\frac{Vcc}{Rc}$

$=\frac{9}{0.5}$

= 0.018 A

VCE =VCC=**9V**

∴ Operating point is(0.018 A,9V)

Q4 A) What is the role of multiplexing in communication system? Explain TDM in detail. (10)

Solution:

Multiplexers, often called muxes, are extremely important to telecommunications. Their main reason for being is to reduce network costs by minimizing the number of communications links needed between two points. As with all other computing systems, multiplexers have evolved. Each new generation has additional intelligence, and additional intelligence brings more benefits. The types of benefits that have accrued, for example, include the following:

The capability to do data compression so that you can encode certain characters with fewer bits than normally required and free up that additional capacity for the movement of other information.

The capability to do error detection and correction between the two points that are being connected to ensure that data integrity and accuracy are being maintained.

The capability to manage transmission resources on a dynamic basis, with such things as priority levels. If you have only one 64Kbps channel left, who gets it? Or what happens when the link between San Francisco and Hong Kong goes down? How else can you reroute traffic to get the high-priority information where it needs to go? Multiplexers help solve such problems.

The more intelligent the multiplexer, the more actively and intelligently it can work on your behalf to dynamically make use of the transmission resources you have.

Time-division multiplexing (TDM

Time-division multiplexing (TDM) is a method of putting multiple data streams in a single signal by separating the signal into many segments, each having a very short duration. Each individual data stream is reassembled at the receiving end based on the timing.

According to sampling theorem, a signal is uniquely specified by its value at intervals(1/2 fm) seconds; where fm is frequency of modulating signal. At receiver the complete signal can be reconstructed from the knowledge of the signal at these instant alone.

During this idle period we may transmit the samples of other signals. We can thus interweave the samples of several signals on the channel. At receiving end, the samples can be seperated by a proper synchronous detector. This is known as Time Division Multiplexing.

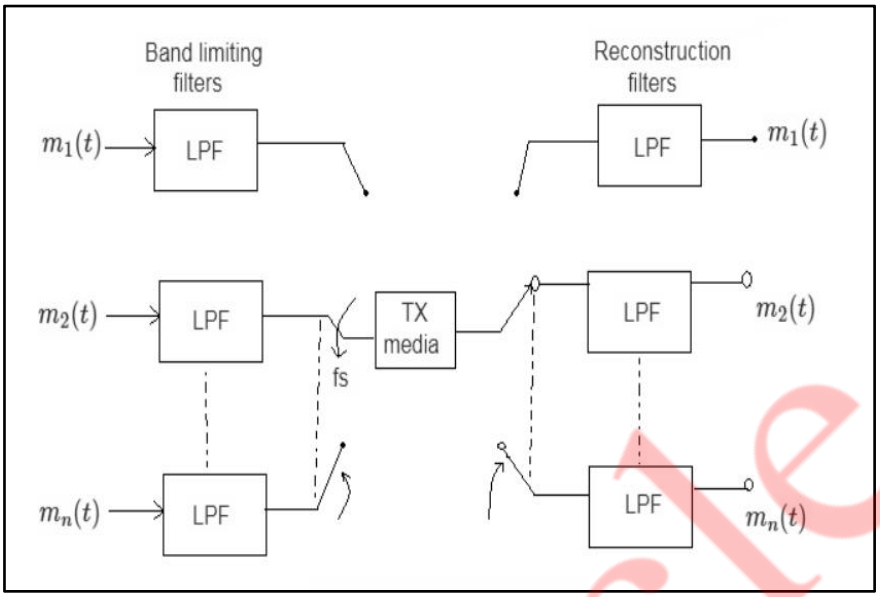


Fig1: Time Division Multiplexing

The switching arrangement at the Tx is provided by the commutator circuit, in each one of its rotation, the commutator extracts or samples, one sample from each message,
input m1(t),m2(t)–––––mn(t)m1(t),m2(t)–––––mn(t)

Thus, at the output of commutator we get PAM waveform which contain the samples of messages input which are periodically inter placed in time.

These multiplexed message samples are transmitted over the communication channel.

At the recovery end decommutator is used which distributes the pulses to different receiver. the decommutator is again a switching arrangement at the receiving end, similar to that of the transmitting end.

This decommutator is used to separate various received samples and to distribute them to an assembly of LPFs. The LPF then re construct the individual
messages, m1(t),m2(t)–––––mn(t)m1(t),m2(t)–––––mn(t) at the output.

Here it is necessary that rate of switching of commutator and decommutator must be same and they must be synchronized to each other, this synchronization is achieved by sending a synchronization pulse.

Thus after sending (n-1) pulses (each pulse from different channels) one synchronization pulse is send, thus overall n pulses are sent in time Ts.

Q4 B) Explain how op-amp can be used as inverting summer. **(10)**

Solution:

Summing amplifier is basically an op-amp that can combine numbers of input signal to a single output that is weighted um of the applied inputs.

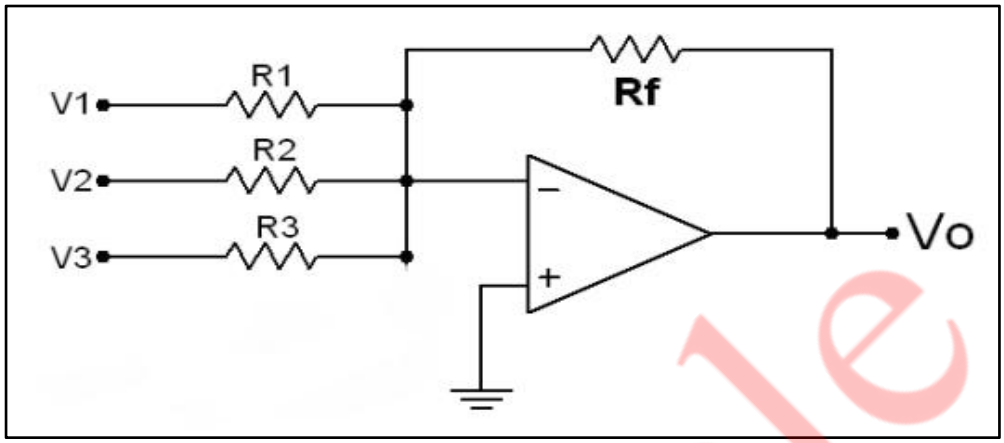


Fig1: Summing inverting amplifier

In this simple summing amplifier circuit, the output voltage, (Vo) now becomes proportional to the sum of the input voltages, V1, V2, V3, etc. Then we can modify the original equation for the inverting amplifier to take account of these new inputs thus:

$$I = -(I_1 + I_2 + I_3)$$

As,

$$I = \frac{v}{R}$$

$$\frac{v_0}{R_f} = -\left(\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3}\right)$$

$$v_0 = -\left[\left(\frac{R_f}{R_1}\right)v_1 + \left(\frac{R_f}{R_2}\right)v_2 + \left(\frac{R_f}{R_3}\right)v_3\right]$$

The above equation is the equation for summing amplifier.

Case 1: If $R_1 = R_2 = R_3 = R_f$ then $v_0 = -(v_1 + v_2 + v_3)$

Therefore, the above circuit works as inverting adder.

Case 2: IF $\frac{R_f}{R_1} \neq \frac{R_f}{R_2} \neq \frac{R_f}{R_3}$ then i/p will be amplified by different scaling factor. Then such an amplifier will be known as scaling amplifier/ scaling adder.

Case 3: If $R_1 = R_2 = R_3 = R_f$ or if $\frac{R_f}{R} = \frac{1}{3}$ then $v_0 = -\left(\frac{v_1+v_2+v_3}{3}\right)$ Such an amplifier will be known as Averaging amplifier.

Q5 A) Derive the formula of total power in AM signal has a total power of 48 Watts with 45% modulation . Calculate the power in the carrier and the sidebands. (10)

Solution:

Carrier power = (Vcarrier x rms)2 / R

= (Vc/ $\sqrt{2}$)2 / R

= Vc 2 /2R

LSB Power = PLSB =[($\frac{mVc}{2}$ / $\sqrt{2}$) / R]2

= m2 Vc2/ 8R

USB Power= m2 Vc2/ 8R

∴ Power in sideband will be PSB= 2 m2 Vc2/ 8R

= m2 Vc2/ 4R

Total power= Pt= Pc + PSB

=Vc 2 /2R + m2 Vc2/ 4R

Pt = Pc(1 + [m2/2])

Given:

Total power (Pt)=48 W

Modulation index (m)= 0.45

Pt = Pc(1 + [m2/2])

48 = Pc (1 + [0.452/2])

Pc=43.59 W

Total power in two sidebands = 48- 43.59

= 4.41 W

So the power in each sidebands = 4.41/2 = 2.205 W

Q5 B) Draw Input and output characteristics of CE configuration. (5)

Solution:

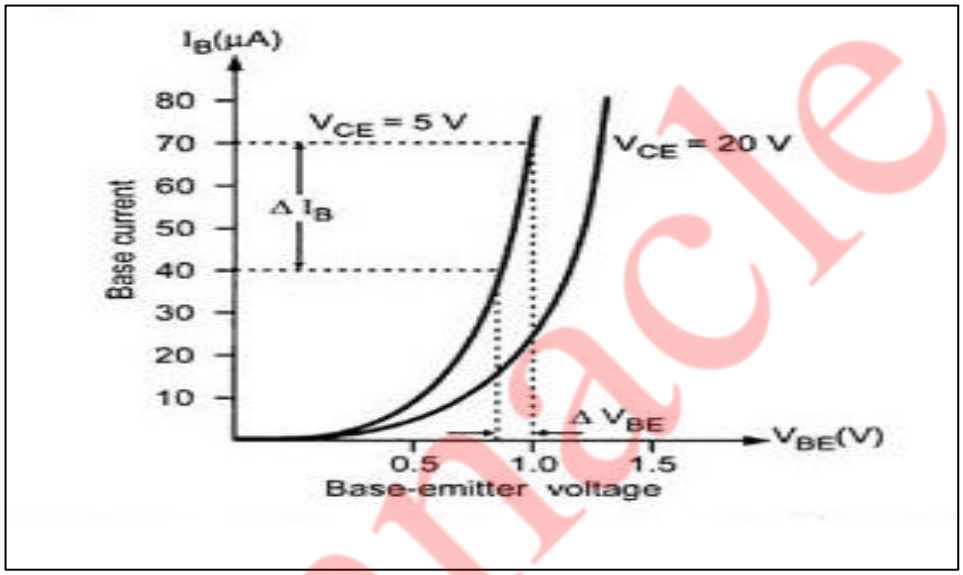


Fig:1 Input characteristics of CE configuration

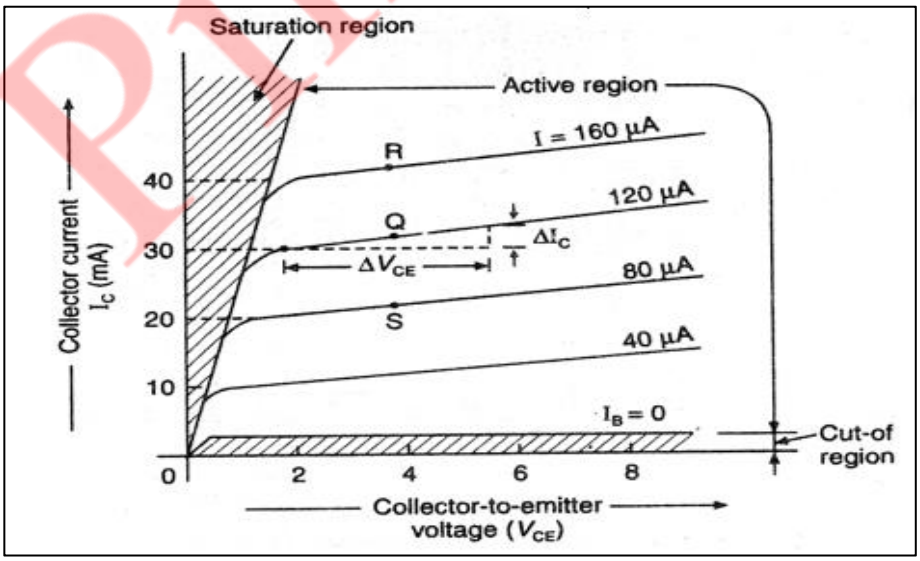


Fig2: Output characteristics of CE configuration

Q5 C) Explain zero crossing detector using op-amp 741. **(5)**

Solution:

The zero-crossing detector (ZCD) circuit is an important application of the op-amp comparator circuit.

A zero-crossing detector is a comparator with the reference level set at zero.

It is used for detecting the zero crossings of AC signals. It can be made from an operational amplifier with an input voltage at its positive input

It can also be called as the sine to square wave converter.

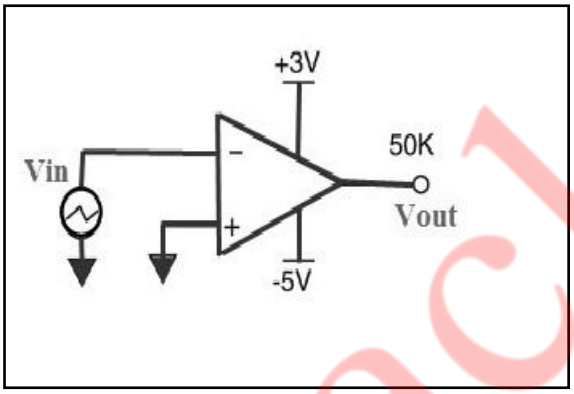


Fig1: Zero crossing detector

Anyone of the inverting or non-inverting comparators can be used as a zero-crossing detector. The only change to be brought in is the reference voltage with which the input voltage is to be compared, must be made zero (Vref = 0V). An input sine wave is given as Vin.

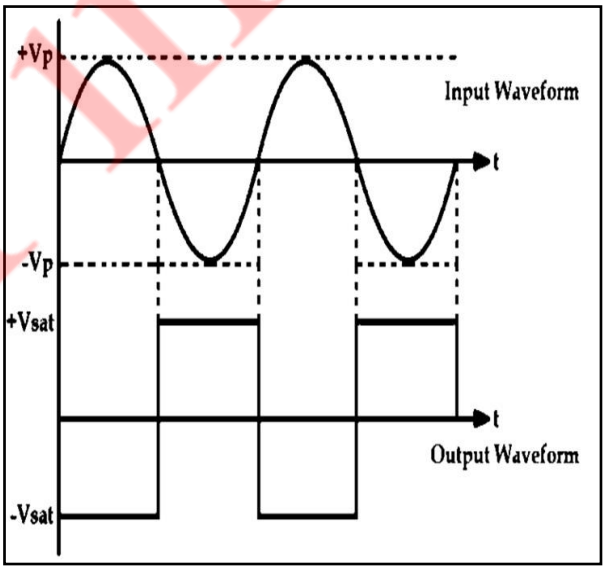


Fig2: Waveform of zero crossing detector

A zero-crossing detector (ZCD) can be built using a 741 operational amplifier IC. One input must be set to zero for the reference voltage, while a sine wave voltage is applied to the other input. As shown in the fig of waveform, When the input sine wave passes through zero in a negative direction, the output voltage is driven into positive saturation. Similarly, as the input passes zero in a positive

direction, the output is driven into negative saturation. This arrangement is also known as a sine to square wave converter.

ZCDs are useful tools for reducing or eliminating electrical noise. Noise produced during switching is proportional to the amplitude of the AC voltage at the switching point; therefore, switching should take place at the voltage's zero crossing to minimise this noise. Effective zero crossing detection can facilitate this function.

The application of Zero Crossing Detector are:

ZCD as Phasemeter

ZCD as Time Marker Generator

Q6 A) Define measures of information. A source puts out one of five possible symbols once every millisecond. The probabilities of these symbols are 1/2, 1/4, 1/8, 1/16 and 1/16. Find information rate and Entropy. (10)

Solution:

measures of information:

Source of communication system is information, which can be analog or digital.

Information theory is a mathematical approach to the study of coding of information along with the quantification, storage, and communication of information.

Hartley defined the first information measure:

H= n log s

Where, n is the length of message and s is the number of possible values for each symbol in the message.

Shannon proposed variant(Shannon's Entropy):

Entropy can be defined as a measure of the average information content per source symbol. Claude Shannon, the "father of the Information Theory", provided a formula for it as −

$$H= \sum Pi \log 2 \quad \frac{1}{Pi}$$

Where pi is the probability of the occurrence of character number i from a given stream of characters and b is the base of the algorithm used. Hence, this is also called as Shannon's Entropy.

$$H= \sum Pi \log 2 \quad \frac{1}{Pi}$$

$$H= \frac{1}{2}\log 2 \quad 2 + \frac{1}{4}\log 2 \quad 4+\frac{1}{8}\log 2 \quad 8+\frac{1}{16}\log 2 \quad 16+\frac{1}{16}\log 2 \quad 16$$

$$H= \frac{1}{2}+\frac{1}{2}+\frac{3}{8}+\frac{1}{4}+\frac{1}{4}$$

H= 1.875 bits/symbol

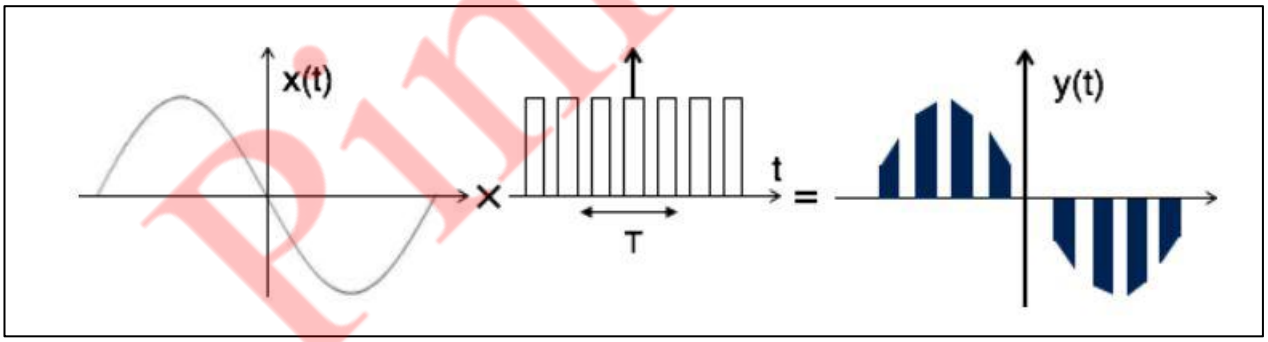
Symbol rate r= fb $= \frac{1}{Tb}$ =1000 symbols/sec

Information rate (R)= rH= 1000 x 1.875= 1875 bits/sec

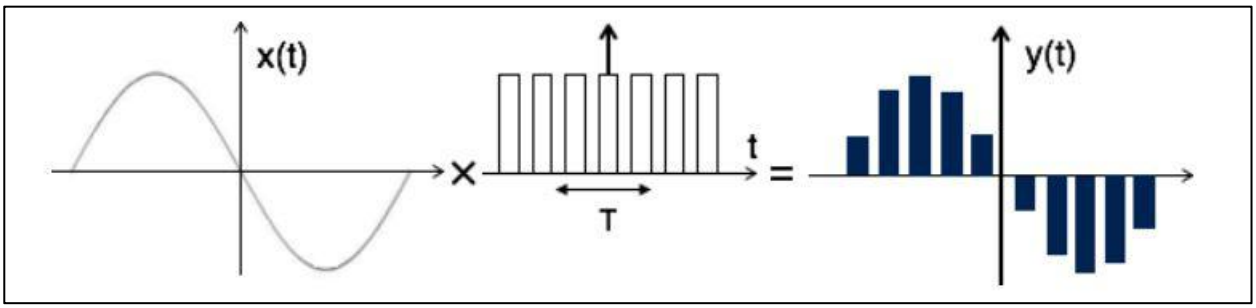
Q6 B) Draw waveforms of natural and flat top sampling signal for a given sine wave signal. (5)

Solution:

Natural Sampling signal



Flat top Sampling



Q6 C) Draw block diagram of super-heterodyne receiver with waveforms for each block. (5)

Solution: